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DETAILED DESCRIPTION

[Detailed explanation of a design]
[0001]
[Industrial Application]
This design is related with a radio set.
[0002]
[Description of the Prior Art]
In recent years, in the radio set, in order to measure the simplification of presetting actuation, the so-called auto preset feature which stores a receivable broadcasting station in storage, such as memory, automatically is adopted.
[0003]
If it is attached to a **** auto preset feature and explains briefly, the microcomputer which manages actuation of a radio set corresponding to actuation of a user's auto preset key will perform automatic scanning actuation. And it is a broadcast signal more than predetermined level as a result of this automatic scanning.
If it ******, a microcomputer will memorize the division ratio corresponding to the frequency concerned to storage, and will resume sweep actuation. By repeating such a procedure, the broadcast signal more than predetermined level is automatically memorized in storage.
[0004]
Moreover, by changing into a digital signal the carrier signal (analog signal) acquired from the input signal, matching the digital information concerned with received frequency information, and memorizing it, field strength level rearranges into descending the contents memorized by the store, and, recently, there is a thing it was made to raise a user's user-friendliness.
[0005]
[Problem(s) to be Solved by the Device]
However, with ** et al. and the above-mentioned configuration, since an A-D converter was needed separately, it was what invites the rise of cost to the increase list of components mark.
[0006]
[Means for Solving the Problem]
While, as for this design, a local oscillation circuit consists of phase-locked loops (PLL) in view of the above-mentioned technical problem An automatic scanning means to be the radio set with which dual gate FET was arranged in the high frequency magnification stage, to start automatic scanning actuation according to a command, and to suspend said automatic scanning actuation according to reception of the broadcast signal more than predetermined level, When automatic scanning actuation of said automatic scanning means stops according to reception of the broadcast signal more than said predetermined level, An electrical-potential-difference supply means to supply the electrical potential difference which changes at a predetermined step to the 2nd gate of said dual gate FET regardless of received frequency, and to control the gain of said dual gate FET, A judgment means to judge the existence of reception of the broadcast signal more than predetermined level based on the input signal amplified by said dual gate

FET on the gain according to the electrical potential difference supplied from this electrical-potential-difference supply means, When having received with this judgment means is judged, it is characterized by providing a storage means to memorize the information about the electrical potential difference which matches with an input signal and is supplied from said electrical-potential-difference supply means, and the rearrangement means which rearranges the contents memorized by this storage means based on the information about said electrical potential difference.

[0007]

[Function]

According to this design, if the broadcast signal more than predetermined level is received by automatic scanning actuation, an electrical potential difference unrelated to the received frequency concerned will be generated at a predetermined step, the 2nd gate of dual gate FET will be supplied, and the gain of this dual gate FET will be defined.

[0008]

Subsequently, when judging whether said received frequency presents more than predetermined level in this defined gain and presenting more than predetermined level, it matches with the received frequency concerned and a storage means is made to memorize the information about said electrical potential difference. Then, that automatic scanning actuation continued throughout the receiving band, and was performed will rearrange the contents memorized by said store based on the information about said electrical potential difference, if it is judged that data were written in all the storage regions of a judgment or said store.

[0009]

[Example]

Drawing 1 is the block diagram showing one example of this design. An antenna and 2 1 An antenna tuning circuit, Dual gate FET by which, as for 3, the output signal from a tuning circuit 2 is supplied to the 1st gate, The resistance to which 4 becomes the load of dual gate FET 3, and 5 A coupling capacitor, The RF amplifying circuit where 6 carries out selection magnification of the received RF signal, the voltage controlled oscillator with which 7 constitutes a phase-locked loop (PLL) circuit (VCO), 8 mixes the RF signal from the RF amplifying circuit 6, and the oscillation signal from VCO7. The mixing circuit which derives a predetermined intermediate frequency signal, the intermediate frequency amplifying circuit where 9 amplifies the intermediate frequency signal from a mixing circuit 8, The detector circuit where 10 detects the intermediate frequency signal from the intermediate frequency amplifying circuit 9, The programmable divider to which 11 carries out N dividing of the oscillation signal from VCO7, The dividing output from this programmable divider is compared with the reference signal from a reference signal generating circuit, and it is constituted from the control circuit which builds in a phase comparator circuit to the extent that the signal according to phase contrast is outputted by the microcomputer. For the phase contrast signal with which 12 was outputted from the control circuit 11, the low pass filter which is supplied and supplies control voltage to VCO7 based on the phase contrast signal concerned, the DC-DC converter with which 13 supplies reference voltage to a low pass filter 12, the resistance from which 14 becomes the load of a low pass filter 12, and 15 are an input signal.

The level detector which judges whether it is more than ****** level, and supplies a detecting signal to a control circuit 11 at the time more than predetermined level, The drop with which 16 displays received frequency based on the signal from a control circuit 11, 17 is arranged on the track from a low pass filter 12 to the 2nd gate of dual gate FET 3. The 1st analog switch controlled by the control signal S1 from a control circuit 11, 18 is arranged on the track from DC-DC converter 13 to the 2nd gate of dual gate FET 3. For the 2nd analog switch controlled by the control signal S2 from a control circuit 11, and 19, as for a capacitor and 21, the resistance for current limiting and 20 are [the key input section and 22] storage, such as memory.

[0010]

Next, actuation is explained with reference to the flow chart of drawing 2 .

[0011]

If the auto preset key of the key input section 21 is operated, after setting the value K of the memory address counter (not shown) for specifying the storage region of storage 22 to "1", a control circuit 11 will make the division ratio set as a programmable divider increase from a current frequency a predetermined number (for example, "1") every, and will start automatic scanning actuation.
[0012]
moreover, **** automatic scanning actuation is continued until the division ratio set as the current programmable divider becomes the same as the division ratio at the time of sweep actuation initiation, and automatic scanning actuation continues throughout a receiving band and is performed namely, -- (step S-1 to S-3).
[0013]
In addition, at this time, it has the control signal S1 from a control circuit 11 to L level, the control signal S2 has H level, and dual gate FET 3 is in the maximum gain condition.
[0014]
And if a certain thing is judged for a received signal level more than predetermined level in a certain frequency and a detecting signal is supplied to a control circuit 11 as a result of a **** automatic scanning, while changing a control signal S1 into H level, changing a control signal S2 into L level and a control circuit's 11 intercepting the track from DC-DC converter 13, the track from a low pass filter 12 is opened (step S-4, S-5).
[0015]
Moreover, after storing temporarily in a buffer register etc. the division ratio previously set as the programmable divider, the value N of the counter for a predetermined electrical-potential-difference setup is set as 1, but the value of this counter supports tuning voltage from a low pass filter 12, and when a counter value is 1, it is set up so that tuning voltage may be set to 1V.
[0016]
And the control circuit 11 is made as [set / as a programmable divider / the division ratio corresponding to the frequency from which the tuning voltage from a low pass filter 12 is set to 1V], when the value of a counter is 1 (step S-6, S-7).
[0017]
Therefore, VCO7 is oscillated on the frequency which becomes settled in the division ratio concerned, and a receiver receives the broadcast signal with which only this oscillation frequency and intermediate frequency differ from each other. On the other hand, the output of this low pass filter 12 is supplied to the 2nd gate of dual gate FET through the 1st analog switch 17. In addition, with an indicator 16, the frequency previously received based on the data memorized by the buffer register etc. is displayed at this time.
[0018]
Then, while setting a control signal S1 as L level and intercepting the electrical-potential-difference supply from a low pass filter 12, the data memorized by the buffer register are again set as a programmable divider, and, subsequently the output of the level detector 15 is judged (step S-8, S-9, S-10).
[0019]
Since the control voltage of 1V is impressed to the 2nd gate of dual gate FET 3 according to an operation of a capacitor 20 at this time, dual gate FET 3 amplifies an input signal on the gain which becomes settled in the control voltage concerned.
[0020]
And if the detecting signal is not outputted from the level detector 15, a control circuit 11 changes the value of a counter into 2, sets up the division ratio corresponding to this value 2, and repeats an above-mentioned procedure while setting a control signal S1 as H level again (step S-11, S-12).
[0021]
On the other hand, if the detecting signal is outputted, a control circuit 11 will make the information list about received frequency memorize the value of said counter to the field of storage specified in the memory address counter mentioned above.

[0022]
Then, while only 1 makes the value of a memory address counter increase, a control circuit 11 changes a control signal S2 into H level, and only a predetermined number makes the division ratio subsequently to a programmable divider set up increase [control circuit] (step S-14 to S-16).
[0023]
In addition, after the number of presetting reaches a predetermined number (7 when it is this example) or the sweep of the receiving band whole region is completed, as for a control circuit 11, a value rearranges the contents of storage into descending based on the value of said counter (step S-18).
[0024]
[Effect of the Device]
While a local oscillation circuit consists of phase-locked loops (PLL) according to this design An automatic scanning means to be the radio set with which dual gate FET was arranged in the high frequency magnification stage, to start automatic scanning actuation according to a command, and to suspend said automatic scanning actuation according to reception of the broadcast signal more than predetermined level, When automatic scanning actuation of said automatic scanning means stops according to reception of the broadcast signal more than said predetermined level, An electrical-potential-difference supply means to supply the electrical potential difference which changes at a predetermined step to the 2nd gate of said dual gate FET regardless of received frequency, and to control the gain of said dual gate FET, A judgment means to judge the existence of reception of the broadcast signal more than predetermined level based on the input signal amplified by said dual gate FET on the gain according to the electrical potential difference supplied from this electrical-potential-difference supply means, A storage means to memorize the information about the electrical potential difference which matches with an input signal and is supplied from said electrical-potential-difference supply means when having received with this judgment means is judged, Since the rearrangement means which rearranges the contents memorized by this storage means based on the information about said electrical potential difference was provided, an AD translation means etc. is not needed according to a rank, but it becomes possible to memorize received frequency in order of field strength moreover, and is practical.

[Translation done.]

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CLAIMS

[Utility model registration claim]
[Claim 1] While a local oscillation circuit consists of phase-locked loops (PLL) An automatic scanning means to be the radio set with which dual gate FET was arranged in the high frequency magnification stage, to start automatic scanning actuation according to a command, and to suspend said automatic scanning actuation according to reception of the broadcast signal more than predetermined level, When automatic scanning actuation of said automatic scanning means stops according to reception of the broadcast signal more than said predetermined level, An electrical-potential-difference supply means to supply the electrical potential difference which changes at a predetermined step to the 2nd gate of said dual gate FET regardless of received frequency, and to control the gain of said dual gate FET, A judgment means to judge the existence of reception of the broadcast signal more than predetermined level based on the input signal amplified by said dual gate FET on the gain according to the electrical potential difference supplied from this electrical-potential-difference supply means, A storage means to memorize the information about the electrical potential difference which matches with an input signal and is supplied from said electrical-potential-difference supply means when having received with this judgment means is judged, The radio set characterized by providing the rearrangement means which rearranges the contents memorized by this storage means based on the information about said electrical potential difference.

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TECHNICAL FIELD

[Industrial Application]
This design is related with a radio set.
[0002]

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PRIOR ART

[Description of the Prior Art]
In recent years, in the radio set, in order to measure the simplification of presetting actuation, the so-called auto preset feature which stores a receivable broadcasting station in storage, such as memory, automatically is adopted.
[0003]
If it is attached to a **** auto preset feature and explains briefly, the microcomputer which manages actuation of a radio set corresponding to actuation of a user's auto preset key will perform automatic scanning actuation. And it is a broadcast signal more than predetermined level as a result of this automatic scanning.
If it ******, a microcomputer will memorize the division ratio corresponding to the frequency concerned to storage, and will resume sweep actuation. By repeating such a procedure, the broadcast signal more than predetermined level is automatically memorized in storage.
[0004]
Moreover, by changing into a digital signal the carrier signal (analog signal) acquired from the input signal, matching the digital information concerned with received frequency information, and memorizing it, field strength level rearranges into descending the contents memorized by the store, and, recently, there is a thing it was made to raise a user's user-friendliness.
[0005]

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EFFECT OF THE INVENTION

[Effect of the Device]
While a local oscillation circuit consists of phase-locked loops (PLL) according to this design An automatic scanning means to be the radio set with which dual gate FET was arranged in the high frequency magnification stage, to start automatic scanning actuation according to a command, and to suspend said automatic scanning actuation according to reception of the broadcast signal more than predetermined level, When automatic scanning actuation of said automatic scanning means stops according to reception of the broadcast signal more than said predetermined level, An electrical-potential-difference supply means to supply the electrical potential difference which changes at a predetermined step to the 2nd gate of said dual gate FET regardless of received frequency, and to control the gain of said dual gate FET, A judgment means to judge the existence of reception of the broadcast signal more than predetermined level based on the input signal amplified by said dual gate FET on the gain according to the electrical potential difference supplied from this electrical-potential-difference supply means, A storage means to memorize the information about the electrical potential difference which matches with an input signal and is supplied from said electrical-potential-difference supply means when having received with this judgment means is judged, Since the rearrangement means which rearranges the contents memorized by this storage means based on the information about said electrical potential difference was provided, an AD translation means etc. is not needed according to a rank, but it becomes possible to memorize received frequency in order of field strength moreover, and is practical.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Device]
However, with ** et al. and the above-mentioned configuration, since an A-D converter was needed separately, it was what invites the rise of cost to the increase list of components mark.
[0006]

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MEANS

[Means for Solving the Problem]
While, as for this design, a local oscillation circuit consists of phase-locked loops (PLL) in view of the above-mentioned technical problem An automatic scanning means to be the radio set with which dual gate FET was arranged in the high frequency magnification stage, to start automatic scanning actuation according to a command, and to suspend said automatic scanning actuation according to reception of the broadcast signal more than predetermined level, When automatic scanning actuation of said automatic scanning means stops according to reception of the broadcast signal more than said predetermined level, An electrical-potential-difference supply means to supply the electrical potential difference which changes at a predetermined step to the 2nd gate of said dual gate FET regardless of received frequency, and to control the gain of said dual gate FET, A judgment means to judge the existence of reception of the broadcast signal more than predetermined level based on the input signal amplified by said dual gate FET on the gain according to the electrical potential difference supplied from this electrical-potential-difference supply means, When having received with this judgment means is judged, it is characterized by providing a storage means to memorize the information about the electrical potential difference which matches with an input signal and is supplied from said electrical-potential-difference supply means, and the rearrangement means which rearranges the contents memorized by this storage means based on the information about said electrical potential difference.
[0007]

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OPERATION

[Function]
According to this design, if the broadcast signal more than predetermined level is received by automatic scanning actuation, an electrical potential difference unrelated to the received frequency concerned will be generated at a predetermined step, the 2nd gate of dual gate FET will be supplied, and the gain of this dual gate FET will be defined.
[0008]
Subsequently, when judging whether said received frequency presents more than predetermined level in this defined gain and presenting more than predetermined level, it matches with the received frequency concerned and a storage means is made to memorize the information about said electrical potential difference. Then, that automatic scanning actuation continued throughout the receiving band, and was performed will rearrange the contents memorized by said store based on the information about said electrical potential difference, if it is judged that data were written in all the storage regions of a judgment or said store.
[0009]

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EXAMPLE

[Example]
Drawing 1 is the block diagram showing one example of this design. An antenna and 2 1 An antenna tuning circuit, Dual gate FET by which, as for 3, the output signal from a tuning circuit 2 is supplied to the 1st gate, The resistance to which 4 becomes the load of dual gate FET 3, and 5 A coupling capacitor, The RF amplifying circuit where 6 carries out selection magnification of the received RF signal, the voltage controlled oscillator with which 7 constitutes a phase-locked loop (PLL) circuit (VCO), 8 mixes the RF signal from the RF amplifying circuit 6, and the oscillation signal from VCO7. The mixing circuit which derives a predetermined intermediate frequency signal, the intermediate frequency amplifying circuit where 9 amplifies the intermediate frequency signal from a mixing circuit 8, The detector circuit where 10 detects the intermediate frequency signal from the intermediate frequency amplifying circuit 9, The programmable divider to which 11 carries out N dividing of the oscillation signal from VCO7, The dividing output from this programmable divider is compared with the reference signal from a reference signal generating circuit, and it is constituted from the control circuit which builds in a phase comparator circuit to the extent that the signal according to phase contrast is outputted by the microcomputer. For the phase contrast signal with which 12 was outputted from the control circuit 11, the low pass filter which is supplied and supplies control voltage to VCO7 based on the phase contrast signal concerned, the DC-DC converter with which 13 supplies reference voltage to a low pass filter 12, the resistance from which 14 becomes the load of a low pass filter 12, and 15 are an input signal.
The level detector which judges whether it is more than ****** level, and supplies a detecting signal to a control circuit 11 at the time more than predetermined level, The drop with which 16 displays received frequency based on the signal from a control circuit 11, 17 is arranged on the track from a low pass filter 12 to the 2nd gate of dual gate FET 3. The 1st analog switch controlled by the control signal S1 from a control circuit 11, 18 is arranged on the track from DC-DC converter 13 to the 2nd gate of dual gate FET 3. For the 2nd analog switch controlled by the control signal S2 from a control circuit 11, and 19, as for a capacitor and 21, the resistance for current limiting and 20 are [the key input section and 22] storage, such as memory.
[0010]
Next, actuation is explained with reference to the flow chart of drawing 2 .
[0011]
If the auto preset key of the key input section 21 is operated, after setting the value K of the memory address counter (not shown) for specifying the storage region of storage 22 to "1", a control circuit 11 will make the division ratio set as a programmable divider increase from a current frequency a predetermined number (for example, "1") every, and will start automatic scanning actuation.
[0012]
moreover, **** automatic scanning actuation is continued until the division ratio set as the current programmable divider becomes the same as the division ratio at the time of sweep actuation initiation, and automatic scanning actuation continues throughout a receiving band and is performed namely, --

(step S-1 to S-3).
[0013]
In addition, at this time, it has the control signal S1 from a control circuit 11 to L level, the control signal S2 has H level, and dual gate FET 3 is in the maximum gain condition.
[0014]
And if a certain thing is judged for a received signal level more than predetermined level in a certain frequency and a detecting signal is supplied to a control circuit 11 as a result of a **** automatic scanning, while changing a control signal S1 into H level, changing a control signal S2 into L level and a control circuit's 11 intercepting the track from DC-DC converter 13, the track from a low pass filter 12 is opened (step S-4, S-5).
[0015]
Moreover, after storing temporarily in a buffer register etc. the division ratio previously set as the programmable divider, the value N of the counter for a predetermined electrical-potential-difference setup is set as 1, but the value of this counter supports tuning voltage from a low pass filter 12, and when a counter value is 1, it is set up so that tuning voltage may be set to 1V.
[0016]
And the control circuit 11 is made as [set / as a programmable divider / the division ratio corresponding to the frequency from which the tuning voltage from a low pass filter 12 is set to 1V], when the value of a counter is 1 (step S-6, S-7).
[0017]
Therefore, VCO7 is oscillated on the frequency which becomes settled in the division ratio concerned, and a receiver receives the broadcast signal with which only this oscillation frequency and intermediate frequency differ from each other. On the other hand, the output of this low pass filter 12 is supplied to the 2nd gate of dual gate FET through the 1st analog switch 17. In addition, with an indicator 16, the frequency previously received based on the data memorized by the buffer register etc. is displayed at this time.
[0018]
Then, while setting a control signal S1 as L level and intercepting the electrical-potential-difference supply from a low pass filter 12, the data memorized by the buffer register are again set as a programmable divider, and, subsequently the output of the level detector 15 is judged (step S-8, S-9, S-10).
[0019]
Since the control voltage of 1V is impressed to the 2nd gate of dual gate FET 3 according to an operation of a capacitor 20 at this time, dual gate FET 3 amplifies an input signal on the gain which becomes settled in the control voltage concerned.
[0020]
And if the detecting signal is not outputted from the level detector 15, a control circuit 11 changes the value of a counter into 2, sets up the division ratio corresponding to this value 2, and repeats an above-mentioned procedure while setting a control signal S1 as H level again (step S-11, S-12).
[0021]
On the other hand, if the detecting signal is outputted, a control circuit 11 will make the information list about received frequency memorize the value of said counter to the field of storage specified in the memory address counter mentioned above.
[0022]
Then, while only 1 makes the value of a memory address counter increase, a control circuit 11 changes a control signal S2 into H level, and only a predetermined number makes the division ratio subsequently to a programmable divider set up increase [control circuit] (step S-14 to S-16).
[0023]
In addition, after the number of presetting reaches a predetermined number (7 when it is this example) or the sweep of the receiving band whole region is completed, as for a control circuit 11, a value rearranges the contents of storage into descending based on the value of said counter (step S-18).

[0024]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing one example of this design.
[Drawing 2] It is the flow chart which shows actuation concerning this design.
[Description of Notations]
3 Dual Gate FET
7 Voltage Controlled Oscillator (VCO)
11 Control Circuit
12 Low Pass Filter
15 Level Detector
17 1st Analog Switch
18 2nd Analog Switch

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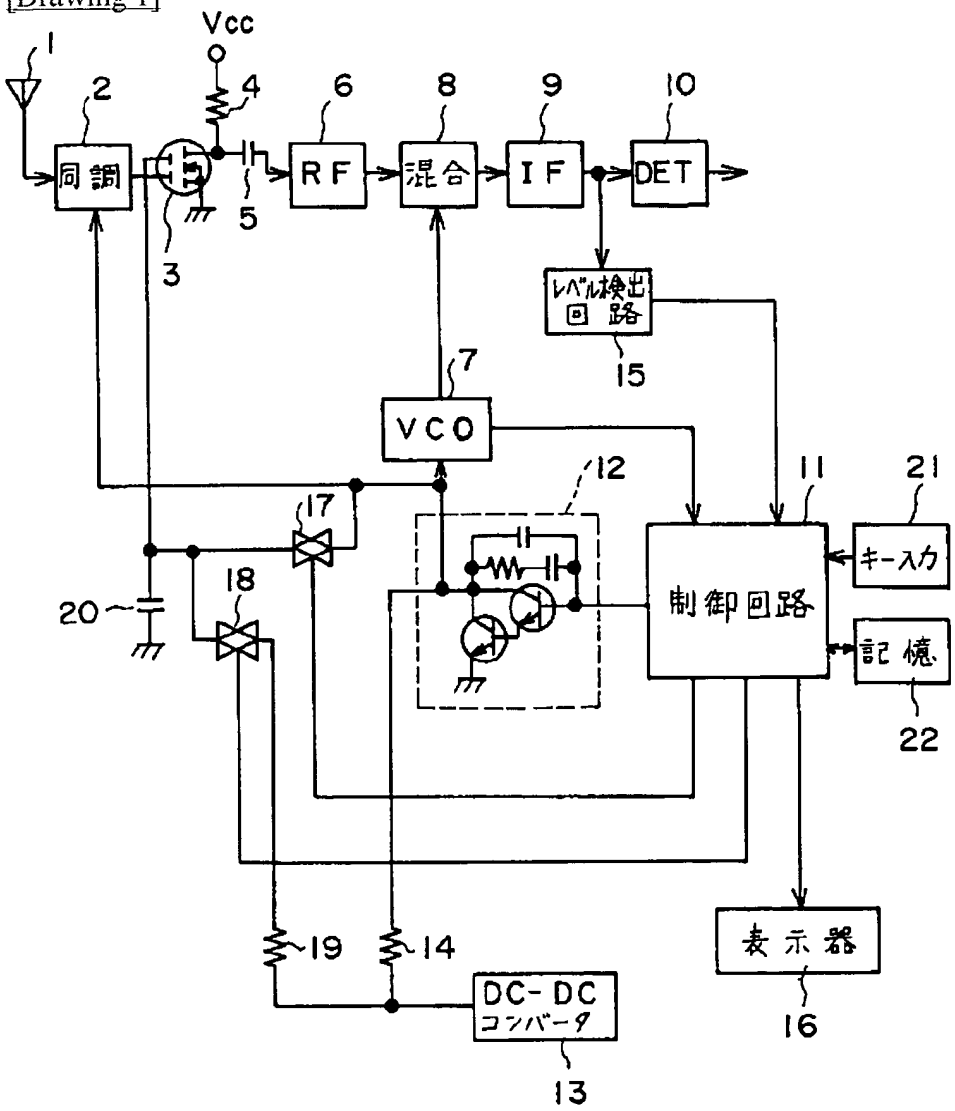
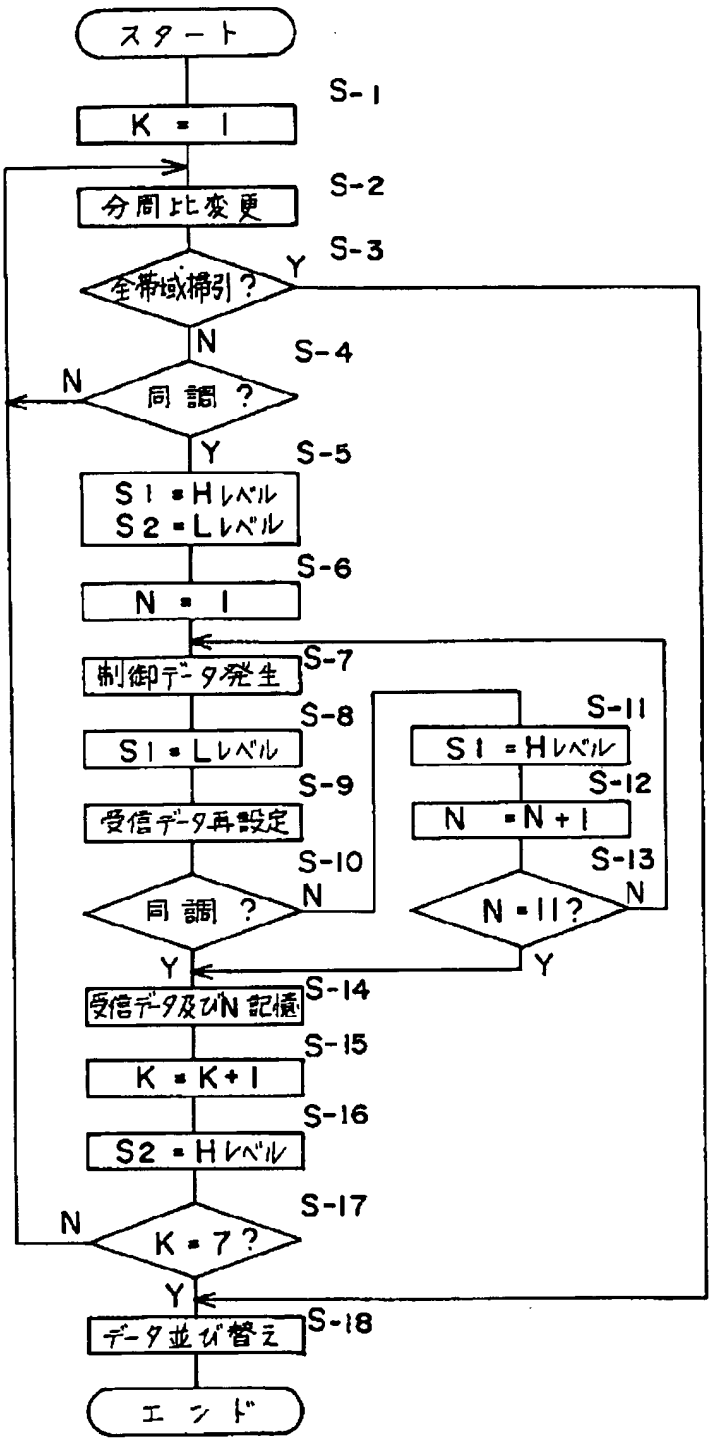
DRAWINGS

[Drawing 1]



[Drawing 2]



[Translation done.]